REMARKS

At the time of the Office Action dated March 25, 2004, claims 1-10 were pending. Applicant acknowledges, with appreciation, the Examiner's indication that claims 3, 4, 6, 9 and 10 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1, 2, 5, 7 and 8 stand rejected.

In this Amendment, claims 1-10 have been amended for better form, but their scopes are not narrowed for any reason relating to patentability. Care has been exercised to avoid the introduction of new matter.

Claims 1-4 and 6 have been objected to.

With respect to claims 1-4, the Examiner pointed out that the recitation "said external input terminals" of claim 1 lacks antecedent basis. In response, Applicant have replaced the recitation with --said external input terminal--. The Examiner also suggested revising claims 2 and 6 as follows: the recitation "a logic level same as the logic level" in claim 2 is replaced with --a logic level the same as the logic level--, and the recitation "the taken a plurality of first data signals" in claim 6 with --the taken plurality of first data signals--. Claims 2 and 6 have been amended in a manner suggested by the Examiner.

Accordingly, withdrawal of the objections to the claims is respectfully solicited.

Claims 1, 2, 5, 7 and 8 have been rejected under 35 U.S.C. §102(b) as being anticipated by Nishimura et al.

In the statement of the rejection, the Examiner asserted that Nishimura et al. discloses a test circuit for logic ICs identically corresponding to what is claimed. This rejection is respectfully traversed.

The factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

Based on the above legal tenet, Applicant submits that the reference does not disclose a semiconductor device including all the limitations recited in claims 1, 2, 5, 7 and 8 within the meaning of 35 U.S.C. §102.

Nishimura et al. discloses flip-flops FFi for holding test control data, and multiplexers Mi for generating control signals Ci based on timing signals to test an arithmetic block LB at high speed. See Abstract.

Applicant first acknowledges, with appreciation, Examiner Charioui's courtesy and professionalism in discussing correspondence of elements recited in claims 1 and 5 to elements in Nishimura et al. in response to Applicant's April 8, 2004 request. With respect to **claim 1**, it is Applicant's understanding that Examiner Charioui identified a data input pin P1 of Nishimura (Fig. 2) as "an external input terminal" of the claimed invention, multiplexers Mi as "a selecting circuit," a bus switch 7 and an arithmetic block LB as a whole as "a plurality of gate circuits," a bus between the bus switch 7 and a data pin P3 as "a signal transmission line," and the data pin P3 as "an external output terminal."

In response, Applicant specifically submits that Nishimura et al. does not disclose a semiconductor device including the "selecting circuit for selecting any of a plurality of internal signals ...," recited in claim 1. The Examiner asserted that the multiplexers Mi correspond to the claimed selecting circuit. However, the reference does not describe that the multiplexers Mi are used to select any of a plurality of internal signals, which is then outputted through corresponding one of the plurality of gate circuits. What Nishimura et al. discloses is that "The multiplexers Mi are controlled by a test mode signal to selectively supply control signals held in the flip-flops FF or control signals for normal operations [to the arithmetic block LB comprising an adder 1, registers 2 and 3, a data inverting circuits 4 and 5, and a buffer 6]" (see column 3, lines 13-16) (emphasis added). These signals are not outputted through the bus switch 7 and the arithmetic block LB to the data pin P3. Nishimura et al. is silent as to selecting any of a plurality of internal signals.

With respect to **claim 5**, it is Applicant's understanding that the Examiner identified a data input pin P1 of Nishimura (Fig. 2) as "an external input terminal" of the claimed invention, multiplexers M as "a first selecting circuit," flip-flops FFi (Fig. 2) as "a signal generating circuit," flip-flops FFi and AND gates G3, G4 and G5 as "a plurality of first gate circuits," and an arithmetic block LB (Fig. 2) as "an internal circuit."

In response, Applicant submits that Nishimura et al. does not specifically disclose a semiconductor device including a "first selecting circuit for selecting one or more of a plurality of first internal signals...," recited in claim 5. The Examiner asserted that the multiplexers Mi correspond to the claimed first selecting circuit. However, for the reasons set forth above, the reference does not describe that the multiplexers Mi are used to select

any of a plurality of internal signals, which is then outputted through corresponding one of the "plurality of first gate circuits." Again, what Nishimura et al. discloses is that "The multiplexers Mi are controlled by a test mode signal to selectively supply control signals held in the flip-flops FF or control signals for normal operations [to the arithmetic block LB comprising an adder 1, registers 2 and 3, a data inverting circuits 4 and 5, and a buffer 6]" (see column 3, lines 13-16) (emphasis added). These signals are not outputted through the bus switch 7 and the arithmetic block LB to the data pin P3. Nishimura et al. is silent as to selecting any of a plurality of internal signals, as claimed.

Applicant further submits that Nishimura et al. does not disclose a "plurality of first gate circuits" responsive to signal selection of the "first selecting circuit." The Examiner identified Nishimura's flip-flops FFi and AND gates G3, G4 and G5 as "a plurality of first gate circuits." However, Nishimura et al. simply discloses about the AND gates G3, G4 and G5 that "The G3, G4 and G5 disposed between the flip-flops FF1, FF2 and FF7 and the multiplexers M1, M2 and M7, respectively, to control the operation timing of the input register A2, input register B3 and output driver 6 of the arithmetic block LB" (emphasis added) (column 3, lines 16-21). By referring to the above cited portion, it is apparent that Nishimura's flip-flops FFi and AND gates G3, G4 and G5 do not correspond to "a plurality of first gate circuits" because those elements cannot operate based on signal selection of the multiplexers M1, M2 and M7, identified as the claimed first selecting circuit by the Examiner.

In addition to the above discussions regarding claims 1 and 5, Applicant further points out differences between the claimed invention and the Nishimura circuit. As an internal bus is used in the Nishimura circuit, a test can be performed only when an

input/output terminal of a test object circuit is connected to the bus. In other words, a test object circuit must have its input/output terminal connected to the bus, or a whole circuit construction thereof must be changed so as to include a bus for the test. In contrast, the claimed invention has no limitation on a bus, and therefore, an arbitrary circuit can be used as a test object circuit without changing a whole circuit contraction (though an additional test circuit is required). Accordingly, the present invention is flexibly adaptable to addition or change of a test object circuit.

In the Nishimura circuit, pins P1, P2 and P3 are required for a test. P1 is a multiple-bit pin (32 bits, for example) because it is connected to a bus. Since multiple-bit pin P1 must be controlled and monitored from the outside of an LSI, it needs many external pins (pins of LSI), which results in an increased cost of an LSI. When a plurality of test object circuits (partial circuits in an LSI) are set, a whole circuit construction must be changed to center a bus as described above, or a plurality of P1 must be provided. As the changing of the circuit centering the bus will be an extensive modification affecting a whole design, it is not flexibly adaptable to addition or change of the test object circuit. In addition, LSI external pins are markedly increased to provide a plurality of P1, which results in a remarkably increased cost of an LSI. In contrast, the claimed invention has no limitation on a bus, and a test can be performed only with an input pin of one bit and an output pin of one bit. Therefore, an increased in the cost resulting from increased pins for test is ignorable.

It is noted that although Fig. 7 of the present Application shows a plurality of output pins, the figure only indicates that a plurality of output pins may be used when increasing the output pins is allowed, and does not mandate use of a plurality of output pins.

Accordingly, the above-described fundamental differences between the claimed invention and Nishimura et al. undermine the factual determination that Nishimura et al. identically describes the claimed invention within the meaning 35 U.S.C. §102. *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc.,* 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Kloster Speedsteel AB v. Crucible Inc.,* 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). Applicant, therefore, respectfully submits that the imposed rejection of independent claims 1 and 5 under 35 U.S.C. §102(b) for lack of novelty as evidenced by Nishimura et al. is not factually viable and, hence, solicits withdrawal thereof.

Applicant notes that a dependent claim is not anticipated if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claim. Therefore, claims 2, 7 and 8 are patentable because they respectively include all the limitations of independent claims 1 and 5. The Examiner's additional comments with respect to claims 2 and 8 do not cure the argued fundamental deficiencies of Nishimura et al. Accordingly, Applicant respectfully solicits withdrawal of the rejection of claims 2, 7 and 8, and favorable consideration thereof.

Applicant further notes that Examiner Charioui pointed out during the above-mentioned discussion that claim 7 is not supported by the specification. In response, Applicant submits that claim 7 is clearly supported by the specification and drawings. For example, a second selecting circuit corresponds to a shift register designating decoder circuit 13 and a group of signal monitoring shift registers 20 in Fig. 1B; a plurality of second gate circuits correspond to tristate buffers 22.1, 22.2, ... in Fig. 1B; a signal transmission line

corresponds to a tristate bus 21 in Fig. 1B; and an external output terminal corresponds to an external output pin 24 in Fig. 1B.

Conclusion.

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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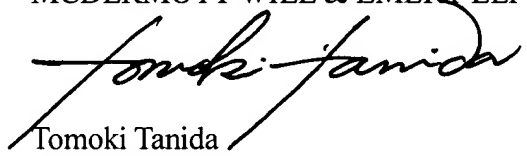

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